



power transition hardware gate | RTL estimate

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A Raghunathan, NK Jha - Computer Design: VLSI in Computers and Processors, 1994. ..., 1994 -
ieeexplore.ieee.org

... to be compatible and can share a hardware resource if ... level power estimation models
[5]. In [5], power dissipation is ... the probability of a transition at each ...

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[book High-Level Power Analysis and Optimization - group of 2 »](#)

A Raghunathan, NK Jha, S Dey - 1997 - books.google.com

... arrays to memories in order to minimize transitions on the ... This resulted in power
management stand- dards for ... The hardware design process is often performed by ...

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[Efficient power estimation techniques for HW/SW systems - group of 7 »](#)

M Lajolo, A Raghunathan, S Dey, L Lavagno, A ... - Low-Power Design, 1999. Proceedings, IEEE Alessandro
Volta ..., 1999 - ieeexplore.ieee.org

... such as signal probabilities, transition probabilities, and ... is to em- ploy a hardware
power estimator on ... use the software power estimation framework described ...

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M Lajolo, A Raghunathan, S Dey - Proceedings of the conference on Design, automation and test ..., 2000 -
portal.acm.org

... for simulating the CFSM transition and returning ... be performed using a hardware power
estimator simulating ... use the software power estimation framework described ...

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[Common-Case Computation: A High-Level Technique for Power and Performance Optimization - group of 14 »](#)

G Lakshminarayana, A Raghunathan, KS Khouri, NK ... - Proceedings of the 36th ACM/IEEE conference on
Design ..., 1999 - doi.ieeecomputersociety.org

... and mutual correlations of state transition conditions [11 ... the algorithmic details
of our power or performance ... RTL circuit augmented with hardware that detects ...

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[Controller-based power management for control-flow intensive designs - group of 2 »](#)

S Dey, A Raghunathan, NK Jha, K Wakabayashi - Computer-Aided Design of Integrated Circuits and Systems,
..., 1999 - ieeexplore.ieee.org

... switching activity, and hence the power consumption, in the ... of state transition
probabilities or transition counts in ... path of another example RTL circuit that ...

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[SCALP: an iterative-improvement-based low-power data path synthesis system - group of 4 »](#)

A Raghunathan, NK Jha - Computer-Aided Design of Integrated Circuits and Systems, ..., 1997 -
ieeexplore.ieee.org

... and is the number of transitions at the ... clock selection, module selection, and hardware
sharing interact ... RTL circuit that is optimized for power consumption. ...

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